

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Chambers	Docket No:	TI-30883
Serial No:	09/902,051	Examiner:	Davidson, Dan
Filed:	7/10/2001	Art Unit:	2651
For:	CMOS DC OFFSET CORRECTION CIRCUIT WITH PROGRAMMABLE HIGH-PASS TRANSFER FUNCTION		

AMENDMENT UNDER 37 C.F.R. § 1.115

Assistant Commissioner For Patents
Washington, DC 20231

Dear Sir:

Responsive to the Office Action mailed December 5, 2005 in connection with the above identified application, Applicants respectfully submit the following amendments and remarks.

IN THE CLAIMS

Claim 1 (currently amended): An offset correction circuit to correct DC offset in accordance with a data rate, comprising:

- a detection circuit to detect a thermal asperity signal; and
- a filter circuit to respond to said thermal asperity signal ~~in accordance with~~ tracking said data rate.

Claim 2 (original): An offset correction circuit, as in Claim 1, wherein said filter circuit affects said DC offset in accordance with said data rate.

Claim 3 (original): An offset correction circuit, as in Claim 1, wherein said filter circuit is a transconductance circuit.

Claim 4 (original): An offset correction circuit, as in Claim 3, wherein said transconductance circuit shunts current in accordance with said data rate.

Claim 5 (original): An offset correction circuit, as in Claim 3, wherein said transconductance circuit includes a FET to shunt current in accordance with said data rate.

Claim 6 (currently amended): A disk drive system for reading and writing information on a disk, comprising:

- a head to read/write information on said disk;
- a preamplifier to amplify said information; and
- a read channel to process said amplified information, said read channel including:
 - an offset correct circuit to correct DC offset in accordance with a data rate, said offset correction circuit including:
 - a detection circuit to detect a thermal asperity signal; and

a filter circuit to respond to said thermal asperity signal in accordance with tracking said data rate.

Claim 7 (original): A disk drive system, as in Claim 6, wherein said filter circuit affects said DC offset in accordance with said data rate.

Claim 8 (original): A disk drive system, as in Claim 6, wherein said filter circuit is a transconductance circuit.

Claim 9 (original): A disk drive system, as in Claim 8, wherein said transconductance circuit shunts current in accordance with said data rate.

Claim 10 (original): A disk drive system, as in Claim 8, wherein said transconductance circuit includes a FET to shunt current in accordance with said data rate.

REMARKS

Claims 1-10 remain in the application for consideration of the Examiner.

Reconsideration and withdrawal of the outstanding rejections are respectfully requested in light of the above amendments and following remarks.

Claims 1-10 were rejected under 35 U.S.C. § 102(e) as being anticipated by Patti.

By the instant amendment, Applicants have amended the claims in accordance with the personal interview with the Examiner on March 22, 2006.

Applicants appreciate the indication from the Examiner that the claim amendments would patentably define over Patti.

Applicants respectfully submit that Claims 1-10 are now allowable.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,
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